

CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (original): A controller area network (CAN) module, comprising:

a plurality of sets of storage elements for storing a plurality of sets of data representing different states of the CAN module.

Claim 2 (currently amended): The CAN module according to claim 1, including:

a first CAN node;

a second CAN node; and

at least one jointly utilized component of the CAN module components whose state is represented by the sets of data stored in said sets of storage elements and are jointly utilized components that can is configured to be connected

alternately to one of said first CAN node and to said second CAN node.

Claim 3 (currently amended): The CAN module according to claim 2, wherein said at least one jointly utilized component ~~is components are normally components a CAN module component~~ whose capacity utilization is low below a capacity utilization threshold when said CAN module component is only connected to a single CAN bus.

Claim 4 (currently amended): The CAN module according to claim 2, wherein said at least one jointly utilized component ~~includes components include a component which ensures that a CAN protocol is adhered to.~~

Claim 5 (currently amended): The CAN module according to claim 2, wherein said sets of storage elements contain a first storage element set and a second storage element set, and including a first multiplexer through which said at least one jointly utilized component ~~components~~ whose state is represented by the sets of data stored in said sets of storage elements can be connected to one of said first storage element set and said second storage element set.

Claim 6 (currently amended): The CAN module according to claim 5, including a second multiplexer connected to said first CAN node and said second CAN node, and through said second multiplexer, said at least one jointly utilized component components can be connected to one of said first CAN node and to said second CAN node.

Claim 7 (currently amended): The CAN module according to claim 6, wherein:

said at least one jointly utilized component components whose state is represented by the sets of data stored in said sets of storage elements are is connected to said first storage element set through said first multiplexer; and

said at least one jointly utilized component is components connected to said first CAN node via said second multiplexer, if, on a part of said first CAN node, a request to access said at least one jointly utilized component components is present.

Claim 8 (currently amended): The CAN module according to claim 6, wherein:

said at least one jointly utilized component components whose state is represented by the sets of data stored in said sets of storage elements is are connected to said second storage element set through said first multiplexer; and

said at least one jointly utilized component components of the CAN module is are connected to said second CAN node through said second multiplexer, if, on a part of said second CAN node, a request to access said at least one jointly utilized component components of the CAN module is present.

Claim 9 (currently amended): The CAN module according to claim 2, wherein possible reactions of said at least one jointly utilized component components to requests on the part of said first CAN node and said second CAN node are determined in advance and buffer-stored until a relevant request occurs.

Claim 10 (original): A controller area network (CAN) module for a microcontroller, the CAN module comprising:

storage elements for storing data representing different states of the CAN module.

Claim 11 (currently amended): A controller area network (CAN) module for a microcontroller, the CAN module comprising: The ~~CAN module according to claim 10, including:~~

storage elements for storing data representing different states of the CAN module;

bit timing logic units, including a first bit timing logic unit and a second bit timing logic unit; and

a logic unit connected between said bit timing logic units and said storage elements, a state of said logic unit is represented by the data stored in said storage elements and said logic unit is a jointly utilized component that can be connected alternately to one of said first bit timing logic unit and to said second bit timing logic unit.

Claim 12 (original): The CAN module according to claim 11, wherein said logic unit has a component which ensures that a CAN protocol is adhered to.

Claim 13 (original): The CAN module according to claim 11, wherein said storage elements contain a first storage element and a second storage element, and including a first multiplexer connected between said storage elements and said

logic unit, said first multiplexer selectively connecting said logic unit to one of said storage elements.

Claim 14 (original): The CAN module according to claim 13, including a second multiplexer connected between said bit timing logic units and said logic unit and selectively connecting the logic unit to one of said bit timing logic units.

Claim 15 (original): The CAN module according to claim 14, wherein:

said logic unit whose state is represented by the data stored in said storage elements is connected to said first storage element through said first multiplexer; and

said logic unit is connected to said first bit timing logic unit through said second multiplexer, if, on a part of said first bit timing logic unit, a request for access to said logic unit is present.

Claim 16 (original): The CAN module according to claim 14, wherein:

said logic unit whose state is represented by the data stored in said storage elements is connected to said second storage element through said first multiplexer; and

said logic unit is connected to said second bit timing logic unit through said second multiplexer, if, on a part of said second bit timing logic unit, a request to access logic unit is present.

Claim 17 (original): The CAN module according to claim 11, wherein possible reactions of said logic unit to requests from said bit timing logic units are determined in advance and buffer-stored until a relevant request occurs.